Semiconductors

AN10032_1

Special Function Registers: Differences between ISP1581 and ISP1582/83

September 2003

Application Note

Rev 1.0

Revision History:

Version	Date	Descriptions	Author
1.0	July 2003	First version	Albert Goh

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1. Introduction

This application note discusses how the Philips Hi-Speed USB interface device ISP1581 is different from the low-power Hi-Speed USB interface devices ISP1582 and ISP1583 in terms of bits and the corresponding functions.

2. Mode Register

Table 2-1: ISP1581 Mode Register

Bit	7	6	5	4	3	2	1	0
Symbol	CLKAON	SNDRSU	GOSUSP	SFRESET	GLINTENA	WKUPCS	reserved	SOFTCT
Reset	0	0	0	0	0	0	-	0
Bus reset	0	0	0	0	unchanged	0	-	unchanged
Access	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W

Table 2-2: ISP1582/83 Mode Register

Bit	15	14	13	12	11	10	9	8
Symbol	TEST2	TEST1	TEST0	reserved			DMA CLKON	VBUSSTAT
Reset	-	-	-	-	-	-	0	-
Bus reset	-	-	-	-	-	-	0	-
Access	R	R	R	R	R	R	R/W	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CLKAON	SNDRSU	GOSUSP	SFRESET	GLINTENA	WKUPCS	PWRON	SOFTCT
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	unchanged	0	0	unchanged
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The first difference is the size of the mode register. In ISP1581, the mode register is a single byte; in ISP1582/83 it is double bytes.

In the ISP1582/83 mode register, bits 15 to 13 are debugging bits, which will show the status of the MODE1, the MODE0 and the BUS_CONF pins at power-on reset. This will reflect the processor mode selected.

TEST2	TEST1	TEST0	Processor Selection
MODE1	MODE0	BUS_CONF	
0	1	0	Multiplexed Address and Data Bus (Split Bus Mode)
0	1	1	Separated Address and Data Bus (Generic Processor Mode)

Bit 9 DMA CLKON is an on-off switch for the supply clock to the DMA circuit. This is useful when operating in power save mode; that is, the DMA circuit will stop completely to save power. This is to cater for bus-powered applications.

Bit 8 VBUSSTAT reflects the V_{BUS} pin status.

Bit 1 PWRON controls the suspend pin output. When set to logic 0 the suspend pin is HIGH when ISP1583 is in the suspend state. Otherwise, the suspend pin is LOW. And when set to logic 1 and only when the device is woken up from the suspend state, there will be a 200 ns active HIGH pulse on the suspend pin. The suspend pin will remain LOW in all other states.

3. OTG Register

Table 3-1: ISP1582/83 OTG Register

Bit	7	6	5	4	3	2	1	0
Symbol	reserved		DP	BSESSVALID	INITCOND	DISCV	VP	OTG
Reset	-	-	0	-	-	0	0	0
Bus reset	-	-	0	-	-	0	0	0
Access	-	-	R/W	R/W	R/W	R/W	R/W	R/W

The OTG register is a new function register, not found in ISP1581. With the OTG register, ISP1582/83 can initiate a Session Request Protocol (SRP) under the On-The-Go (OTG) specification.

Bit 5, DP, pulses pin DP of the ISP1582/83. The DP pin reflects the status of bit DP.

Bit 4, BSESSVALID, indicates whether a B-session is valid. This bit is latched to logic 1 once V_{BUS} exceeds the B-device session valid threshold. Once set, it remains at logic 1. To clear this bit, write logic 1. (The ISP1583 continuously updates this bit to logic 1 when the B-session is valid. If the B-session is valid after it is cleared, it is set back to logic 1 by the ISP1583).

A status bit of logic 0 implies that the SRP has failed. To proceed to a normal operation, the device can restart the SRP, clear the OTG bit, or proceed to an error handling process. With logic 1, the device clears the OTG bit, goes into the normal operation mode, and sets the SOFTCT bit (DP pull up) in the Mode register. The OTG host has a maximum of 5 seconds before it responds to a session request. During this period, the ISP1582/83 may request to suspend operation. Therefore, the device firmware must wait for some time if it wishes to know the SRP result ('success' when there is minimum response from the host within 5 seconds, and 'failure' when there is no response from the host within 5 seconds).

Bit 3 INIT where writing logic 1 clear this bit. The device clears this bit and waits for more than 2 ms to check the bit status. If it reads logic 0, it means that V_{BUS} remains lower than 0.8 V and DP/DM at SE0 during the elapsed time from the time it is cleared. The device can then start a B-device SRP. If it reads logic 1, it means that the initial condition of an SRP is violated; therefore, the device should abort SRP. The bit is set to logic 1 by the ISP1582/83 when initial conditions are not met, and only writing logic 1 clears the bit. (If initial conditions are not met after this bit has been cleared, it will set again).

Bit 2, DISCV, is set to discharge V_{BUS}. The device discharges V_{BUS} before starting a new SRP. The discharge can take as long as 30 ms for the V_{BUS} to be charged less than 0.8 V. This bit must be cleared before detecting session end.

Bit 1 VP is the V_{BUS} pulsing bit, which will reflect the logic status of the VP. This bit must be set for more than 16 ms and must be cleared before 26 ms.

Bit OTG enables and disables ISP1582/83's OTG function block. By enabling the OTG function, the V_{BUS} sensing pin of ISP1582/83 will not function. Therefore, the V_{BUS} sensing pin can only be used when OTG is not enabled.

The ISP1582 can initiate an SRP. The B-device initiates SRP by data-line pulsing followed by V_{BUS} pulsing. The A-device can detect either data-line pulsing or V_{BUS} pulsing.

The ISP1582 can initiate the B-device SRP by performing the following steps:

1.Detect initial conditions [read INITCOND (bit 3) of the OTG register].

2. Start data-line pulsing [set DP (bit 5) of the OTG register to logic 1].

3. Wait for 5 ms to 10 ms.

4. Stop data-line pulsing [set DP (bit 5) of the OTG register to logic 0].

5. Start V_{BUS} pulsing [set VP (bit 1) of the OTG register to logic 1].

6. Wait for 10 ms to 20 ms.

7. Stop V_{BUS} pulsing [set VP (bit 1) of the OTG register to logic 0].

8. Discharge V_{BUS} for about 30 ms [by using DISCV (bit 2) of the OTG register], optional.
9. Detect BSESSVALID (bit 4) of the OTG register for a successful SRP.

The B-device must complete both data-line pulsing and V_{BUS} pulsing within 100 ms.

When disabling, OTG data-line pulsing bit DP and V_{BUS} pulsing bit VP must be cleared by writing logic 1.

3.1. Interrupt Enable Register

Table 3-2: ISP1581 Interrupt Enable Register

Bit	31	30	29	28	27	26	25	24
Symbol	reserved						IEP7TX	IEP7RX
Reset	-	-	-	-	-	-	0	0
Bus Reset	-	-	-	-	-	-	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	IEP6TX	IEP6RX	IEP5TX	IEP5RX	IEP4TX	IEP4RX	IEP3TX	IEP3RX
Reset	0	0	0	0	0	0	0	0
Bus Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	IEP2TX	IEP2RX	IEP1TX	IEP1RX	IEP0TX	IEP0RX	reserved	IEP0SETUP
Reset	0	0	0	0	0	0	-	0
Bus Reset	0	0	0	0	0	0	-	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved	IEDMA	IEHS_STA	IERESM	IESUSP	IEPSOF	IESOF	IEBRST
Reset	-	0	0	0	0	0	0	0
Bus Reset	-	0	0	0	0	0	0	unchanged
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 3-3: ISP1582/83 Interrupt Enable Register

Bit	31	30	29	28	27	26	25	24
Symbol	reserved						IEP7TX	IEP7RX
Reset	-	-	-	-	-	-	0	0
Bus Reset	-	-	-	-	-	-	0	0
Access	-	-	-	-	-	-	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	IEP6TX	IEP6RX	IEP5TX	IEP5RX	IEP4TX	IEP4RX	IEP3TX	IEP3RX
Reset	0	0	0	0	0	0	0	0
Bus Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	IEP2TX	IEP2RX	IEP1TX	IEP1RX	IEP0TX	IEP0RX	reserved	IEP0SETUP
Reset	0	0	0	0	0	0	-	0
Bus Reset	0	0	0	0	0	0	-	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	IEVBUS	IEDMA	IEHS_STA	IERESM	IESUSP	IEPSOF	IESOF	IEBRST
Reset	0	0	0	0	0	0	0	0
Bus Reset	0	0	0	0	0	0	0	unchanged
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The only difference in the interrupt enable register is bit 7. It is a reserved bit in ISP1581. In ISP1582/83, it is the V_{BUS} detection interrupt enabling bit. Setting bit 7 to logic 1 allows an interrupt to be generated on the INT when there is a V_{BUS} present. Interrupt will not be generated when V_{BUS} is removed. The V_{BUS} interrupt can be used in combination with the V_{BUS} bit in the interrupt register.

3.2. Control Function Register

Table 3-4: ISP1581 Control Function Register

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			CLBUF	VENDP	reserved	STATUS	STALL
Reset	-	-	-	0	0	-	0	0
Bus reset	-	-	-	0	0	-	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 3-5: ISP1582/83 Control Function Register

Bit	7	6	5	4	3	2	1	0
Symbol	reserved			CLBUF	VENDP	DSEN	STATUS	STALL
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit 2 of ISP1581 is reserved. In ISP1582/83, it is the data stage enable bit, used to signify that ISP1582/83 is in data stage for the control pipe. This bit controls the response of the ISP1582 to a control transfer. When this bit is set, the ISP1582 goes to the data stage; otherwise, the ISP1582 will NAK the data stage transfer until the firmware

explicitly responds to the setup command. In case of a control write transfer without the data stage, the OUT endpoint data stage should be set before the IN endpoint status stage bit is set.

Next, the STATUS bit of ISP1581 when enabled will generate an interrupt signal on the INT pin. In ISP1582/83 the STATUS bit will not generate an interrupt, reducing the overhead in the status stage of ISP1582/83 control pipe.

Refer to the application note *Control Pipe of ISP1582/83*.

3.3. Buffer Status Register

Table 3-6: ISP1582/83 Buffer Status Register

Bit	7	6	5	4	3	2	1	0
Symbol	reserved						BUF1	BUF0
Reset	-	-	-	-	-	-	0	0
Bus reset	-	-	-	-	-	-	0	0
Access	-	-	-	-	-	-	R	R

Table 3-7: ISP1582/83 Buffer Status Register: bit description

Bit	Symbol	Description
7 to 2	-	reserved
1 to 0	BUF[1:0]	**00** — The buffers are not filled.
		01 — One of the buffers is filled.
		10 — One of the buffers is filled.
		11 — Both the buffers are filled.

Buffer status register is a new register, which is not implemented in ISP1581. It indicates to the user whether there is data in FIFO. Logic zero in the truth table indicates that the buffer is not filled.

3.4. DMA Command Register

Table 3-8: ISP1581 DMA Command Register

Bit	7	6	5	4	3	2	1	0
Symbol	DMA_CMD[7:0]							
Reset	FFH							
Bus reset	FFH							
Access	W							

Table 3-9: ISP1581 DMA Commands

Code (Hex)	Name	Description
11	Reset DMA	**Reset DMA:** Initializes the DMA core to its power-on reset state. **Remark:** When the DMA core is reset during the Reset DMA command, the DREQ, DACK, DIOW and DIOR handshake pins will be temporarily asserted. This can cause some confusion to the external DMA Controller. To prevent this from happening, start the external DMA Controller **only after** the DMA reset is done.
12	MDMA stop	**MDMA stop:** This command immediately stops the MDMA data transfer. This is applicable for commands 06H and 07H only.
13 to FF	-	reserved

Table 3-10: ISP1582/83 DMA Command Register

Bit	7	6	5	4	3	2	1	0
Symbol	DMA_CMD[7:0]							
Reset	1	1	1	1	1	1	1	1
Bus reset	1	1	1	1	1	1	1	1
Access	W	W	W	W	W	W	W	W

Table 3-11: ISP1582/83 DMA Command

Code (hex)	Name	Description
00	GDMA Read	**Generic DMA IN token transfer (slave mode only):** Data is transferred from the external DMA bus to the internal buffer. Strobe: DIOW by external DMA Controller.
01	GDMA Write	**Generic DMA OUT token transfer (slave mode only):** Data is transferred from the internal buffer to the external DMA bus. Strobe: DIOR by external DMA Controller.
02 to 05	-	reserved
06	MDMA Read	**Multiword DMA Read:** Data is transferred from the external DMA bus to the internal buffer.
07	MDMA Write	**Multiword DMA Write:** Data is transferred from the internal buffer to the external DMA bus.
0A	Read 1F0	**Read at address 01F0H:** Initiates a PIO Read cycle from Task File 1F0. Before issuing this command, the task file byte count should be programmed at address 1F4H (LSB) and 1F5H (MSB).
0B	Poll BSY	**Poll BSY status bit for ATAPI device:** Starts repeated PIO Read commands to poll the BSY status bit of the ATAPI device. When BSY = 0, polling is terminated and an interrupt is generated. The interrupt can be masked but the interrupt bit will still be set. Therefore, you can manually poll this interrupt bit.
0C	Read Task Files	**Read Task Files:** Reads all task files. When Task File Index is set to logic 0, this command reads all registers, except 1F0H and 1F7H. If Task File Index is not logic 0, the Task register of the address set in the Task File register will be read. When the reading is completed, an interrupt is generated. The interrupt could be masked off, however, the interrupt bit will still be set. Therefore, you can manually poll this interrupt bit.

Code (hex)	Name	Description
0D	-	reserved
0E	Validate Buffer	**Validate Buffer (for debugging only):** Request from the microcontroller to validate the endpoint buffer following an ATA to USB data transfer.
0F	Clear Buffer	**Clear Buffer:** Request from the microcontroller to clear the endpoint buffer after a USB to ATA data transfer.
10	Restart	**Restart:** Request from the microcontroller to move the buffer pointers to the beginning of the endpoint FIFO.
11	Reset DMA	**Reset DMA:** Initializes the DMA core to its power-on reset state. **Remark:** When the DMA core is reset during the Reset DMA command, the DREQ, DACK, DIOW and DIOR handshake pins will be temporarily asserted. This can confuse the external DMA Controller. To prevent this, start the external DMA Controller **only after** the DMA reset.
12	MDMA stop	**MDMA stop:** This command immediately stops the MDMA data transfer. This is applicable for commands 06H and 07H only.
13	GDMA stop	**GDMA stop**: This command stops the GDMA data transfer. Any data in the OUT endpoint that is not transferred by the DMA will remain in the buffer. The FIFO data for the IN endpoint will be written to the endpoint buffer. An interrupt bit will be set to indicate the completion of the DMA Stop command.
14 to 20	-	reserved
21	Read Task File register 0x1F1	**Read Task File register 0x1F1**: When reading has been completed, an interrupt is generated.
22	Read Task File register 0x1F2	**Read Task File register 0x1F2**: When reading has been completed, an interrupt is generated.
23	Read Task File register 0x1F3	**Read Task File register 0x1F3**: When reading has been completed, an interrupt is generated.
24	Read Task File register 0x1F4	**Read Task File register 0x1F4**: When reading has been completed, an interrupt is generated.
25	Read Task File register 0x1F5	**Read Task File register 0x1F5**: When reading has been completed, an interrupt is generated.
26	Read Task File register 0x1F6	**Read Task File register 0x1F:**. When reading has been completed, an interrupt is generated.
27	Read Task File register 0x3F6	**Read Task File register 0x3F6**: When reading has been completed, an interrupt is generated.
28	Read Task File register 0x3F7	**Read Task File register 0x3F7**: When reading has been completed, an interrupt is generated.
29 to FF	-	reserved

Additional commands have been added to the DMA command register of the ISP1582/83.

Command GDMA STOP is to stop the GDMA data transfer. Any data in the OUT endpoint that is not transferred by the DMA will remain in the buffer. The FIFO data for the IN endpoint will be written to the endpoint buffer. An interrupt bit will be set to indicate the completion of the DMA stop command.

Commands READ TASK FILE REGISTER 0x1F1 to 0x3F7 are issued to the ISP1583 to selectively update its task file register, as the entire register is not required at every single moment

3.5. DMA Configuration Register

Table 3-12: ISP1581 DMA Configuration Register

Bit	15	14	13	12	11	10	9	8
Symbol	reserved	IGNORE_IORDY	ATA_MODE	DMA_MODE[1:0]		PIO_MODE[2:0]		
Reset	-	0	0	00H		00H		
Bus Reset	-	0	0	00H		00H		
Access	R/W	R/W	R/W	R/W		R/W		
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DIS_XFER_CNT	BURST[2:0]			MODE[1:0]		reserved	WIDTH
Reset	0	00H			00H		-	1
Bus Reset	0	00H			00H		-	1
Access	R/W	R/W			R/W		R/W	R/W

Table 3-13: ISP1582 DMA Configuration Register

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Bus Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DIS_XFER_CNT	reserved			MODE[1:0]		reserved	WIDTH
Reset	0	0	0	0	0	0	0	1
Bus Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 3-14: ISP1583 DMA Configuration Register

Bit	15	14	13	12	11	10	9	8
Symbol	reserved	IGNORE_READY	ATA_MODE	DMA_MODE[1:0]		PIO_MODE[2:0]		
Reset	0	0	0	0	0	0	0	0
Bus Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	DIS_XFER_CNT	reserved			MODE[1:0]		reserved	WIDTH
Reset	0	0	0	0	0	0	0	1
Bus Reset	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The ISP1581 supports burst mode in the DMA configuration, indicated by bits 6 to 4 in the DMA Configuration register. ISP1582/83 also supports burst mode in the DMA configuration, but is now indicated in a separate register, the DMA Burst Counter register.

3.6. DMA Burst Counter Register

Table 3-15: ISP1582/83 DMA Burst Counter Register

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			BURSTCOUNTER[12:8]				
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	-	-	-	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BURSTCOUNTER[7:0]							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

This register defines the burst length. Make the counter a multiple of two in the 16-bit mode. Make the burst counter a multiple of the buffer counter. For the IN endpoint, when burst counter equals 0, in the GDMA mode, DREQ will drop the last cycle when the buffer is full.

3.7. DMA Hardware Register

Table 3-16: ISP1581 DMA Hardware Register

Bit	7	6	5	4	3	2	1	0
Symbol	ENDIAN[1:0]		EOT_POL	MASTER	ACK_POL	DREQ_POL	WRITE_POL	READ_POL
Reset	00H		0	0	0	1	0	0
Bus reset	00H		0	0	0	1	0	0
Access	R/W		R/W	R/W	R/W	R/W	R/W	R/W

Table 3-17: ISP1582 DMA Hardware Register

Bit	7	6	5	4	3	2	1	0
Symbol	ENDIAN[1:0]		EOT_POL	reserved	ACK_POL	DREQ_POL	WRITE_POL	READ_POL
Reset	0	0	0	0	0	1	0	0
Bus reset	0	0	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 3-18: ISP1583 DMA Hardware Register

Bit	7	6	5	4	3	2	1	0
Symbol	ENDIAN[1:0]		EOT_POL	MASTER	ACK_POL	DREQ_ POL	WRITE_ POL	READ_ POL
Reset	0	0	0	0	0	1	0	0
Bus reset	0	0	0	0	0	1	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

In ISP1581, bit 4 is the MASTER bit, used to select the DMA master/slave mode. Logic 0 switches the ISP1581 to GDMA slave mode. Logic 1 switches ISP1581 to the MDMA master mode. These hold for the ISP1583 too.

In ISP1582 the MASTER bit is removed because ISP1582 can be configured only as a GDMA slave.

3.8. DMA Interrupt Reason Register

Table 3-19: ISP1581 DMA Interrupt Reason Register

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			ODD_IND	EXT_EOT	INT_EOT	INTRQ_ PENDING	DMA_ XFER_OK
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	1F0_WF_E	1F0_WF_F	1F0_RF_E	READ_1F0	BSY_ DONE	TF_RD_ DONE	CMD_ INTRQ_OK	reserved
Reset	0	0	0	0	0	0	0	-
Bus reset	0	0	0	0	0	0	0	-
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 3-20: ISP1582 DMA Interrupt Reason Register

Bit	15	14	13	12	11	10	9	8
Symbol	TEST3	reserved		GDMA_ STOP	EXT_EOT	INT_EOT	reserved	DMA_ XFER_OK
Reset	-	-	-	0	0	0	-	0
Bus reset	-	-	-	0	0	0	-	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved							
Reset	-	-	-	-	-	-	-	-
Bus reset	-	-	-	-	-	-	-	-
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 3-21: ISP1583 DMA Interrupt Reason Register

Bit	15	14	13	12	11	10	9	8
Symbol	TEST3	reserved		GDMA_ STOP	EXT_EOT	INT_EOT	INTRQ_ PENDING	DMA_ XFER_OK
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	1F0_WF_E	1F0_WF_F	1F0_RF_E	READ_1F0	BSY_ DONE	TF_RD_ DONE	CMD_ INTRQ_OK	reserved
Reset	0	0	0	0	0	0	0	-
Bus reset	0	0	0	0	0	0	0	-
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

ISP1581's bit 12 ODD_IND has been replaced in ISP1582/83 by GDMA_STOP. When the GDMA_STOP command is issued to the DMA Command registers, it means the DMA transfer has successfully terminated.

In ISP1582, bit 9 and the register's lower byte are reserved because ISP1582 supports only GDMA slave mode.

3.9. DMA Interrupt Enable Register

Table 3-22: ISP1581 DMA Interrupt Enable Register

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			IE_ODD _IND	IE_EXT_EOT	IE_INT_EOT	IE_INTRQ_ PENDING	IE_DMA_ XFER_OK
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	IE_1F0_ WF_E	IE_1F0_ WF_F	IE_1F0_ RF_E	IE_ READ_1F0	IE_BSY_ DONE	IE_TF_ RD_DONE	IE_CMD_ INTRQ_OK	reserved
Reset	0	0	0	0	0	0	0	-
Bus reset	0	0	0	0	0	0	0	-
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 3-23: ISP1582 DMA Interrupt Enable Register

Bit	15	14	13	12	11	10	9	8
Symbol	TEST4	reserved		IE_GDMA_ STOP	IE_EXT_ EOT	IE_INT_ EOT	reserved	IE_DMA_ XFER_OK
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	R	-	-	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 3-24: ISP1583 DMA Interrupt Enable Register

Bit	15	14	13	12	11	10	9	8
Symbol	TEST4	reserved		IE_GDMA_STOP	IE_EXT_EOT	IE_INT_EOT	IE_INTRQ_ENDING	IE_DMA_XFER_OK
Reset	-	-	-	0	0	0	0	0
Bus reset	-	-	-	0	0	0	0	0
Access	R	-	-	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	IE_1F0_WF_E	IE_1F0_WF_F	IE_1F0_RF_E	IE_READ_1F0	IE_BSY_DONE	IE_TF_RD_DONE	IE_CMD_INTRQ_OK	reserved
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The GDMA_STOP interrupt enable bit in the ISP1582/83 replaces ISP1581's bit 12 ODD_IND interrupt. When the GDMA_STOP command is issued to the DMA Command registers, it means the DMA transfer has successfully terminated.

ISP1582's BIT 9 and the lower byte of the register are reserved because ISP1582 supports only GDMA slave mode.

3.10. Interrupt Register

Table 3-25: ISP1581 Interrupt Register

Bit	31	30	29	28	27	26	25	24
Symbol	reserved						EP7TX	EP7RX
Reset	-	-	-	-	-	-	0	0
Bus reset	-	-	-	-	-	-	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	23	22	21	20	19	18	17	16
Symbol	EP6TX	EP6RX	EP5TX	EP5RX	EP4TX	EP4RX	EP3TX	EP3RX
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	15	14	13	12	11	10	9	8
Symbol	EP2TX	EP2RX	EP1TX	EP1RX	EP0TX	EP0RX	reserved	EP0SETUP
Reset	0	0	0	0	0	0	-	0
Bus reset	0	0	0	0	0	0	-	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	reserved	DMA	HS_STAT	RESUME	SUSP	PSOF	SOF	BRESET
Reset	-	0	0	0	0	0	0	0
Bus reset	-	0	0	0	0	0	0	unchanged
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 3-26: ISP1582/83 Interrupt Register

Bit	31	30	29	28	27	26	25	24
Symbol	reserved						EP7TX	EP7RX
Reset	-	-	-	-	-	0	0	0
Bus reset	-	-	-	-	-	0	0	0
Access	-	-	-	-	-	R/W	R/W	R/W
Bit	**23**	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Symbol	EP6TX	EP6RX	EP5TX	EP5RX	EP4TX	EP4RX	EP3TX	EP3RX
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	EP2TX	EP2RX	EP1TX	EP1RX	EP0TX	EP0RX	reserved	EP0SETUP
Reset	0	0	0	0	0	0	-	0
Bus reset	0	0	0	0	0	0	-	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	-	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VBUS	DMA	HS_STAT	RESUME	SUSP	PSOF	SOF	BRESET
Reset	0	0	0	0	0	0	0	0
Bus reset	0	0	0	0	0	0	0	unchanged
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The only difference in the interrupt register is bit 7. In ISP1581 it is reserved; in ISP1582/83 it is a V_{BUS} interrupt status bit. V_{BUS} status is set to logic 1 when V_{BUS} is present and the interrupt generated is based on the interrupt enable register.

4. References

- *Universal Serial Bus Specification Rev. 2.0*
- *ISP1581 Hi-Speed Universal Serial Bus interface device* data sheet
- *ISP1582 Hi-Speed Universal Serial Bus interface device* data sheet
- *ISP1583 Hi-Speed Universal Serial Bus interface device* data sheet
- *Control Pipe of ISP1582/83* application note

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